REMARKS

Claims 1-7 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,648,300 to Nakayama et al. In this regard, the Examiner considered Nakayama et al as meeting each of the terms of the rejected claims.

Applicants traverse, and respectfully request the Examiner to reconsider for the following reasons.

Nakayama et al illustrates a method of manufacturing a cantilever drive mechanism, including a process of forming a processing circuit portion, an ensuing process of forming the cantilever portion, a process of forming a micro-tip, and a process of removing the substrate (col. 7, lines 41-44). The Examiner cited those portions of Nakayama et al concerning fabrication of the NMOS device (i.e., part of the processing circuit portion), but this has nothing to do with fabricating micro-tip 11 of Nakayama et al properly corresponding to the semiconductor probe of the present claims. As shown in Fig. 1 of Nakayama et al, micro-tip 11 for detecting a tunnel current is electrically connected to the NMOS transistor (i.e., part of the processing circuit portion), which drives the cantilever portion and detects and amplifies the tunnel current (col. 3, lines 40-51).

The micro-tip 11 of Nakayama et al is preferably formed from a noble metal such as Au, Pt and Pd (col. 9, lines 10-11), and therefore is entirely different from the corresponding semiconductor probe of the present claims including a tip doped with first impurities formed on an end portion of the cantilever, and a resistive region lightly doped with second impurities formed at a peak of the tip. Nowhere does Nakayama et al disclose fabricating a semiconductor probe as defined in present claim 1. For this reason alone, it is respectfully submitted that the present claims define novel subject matter.

With respect to the method steps of present claim 1, Nakayama et al fails to disclose step (c) which comprises patterning a mask layer and etching a portion of a top surface of the substrate not covered by the patterned mask layer *to form a resistive tip*. For this additional reason, it is respectfully submitted that Nakayama et al fails to anticipate the present claims.

With respect to present claim 2, Nakayama et al surely teaches an annealing step. However, nowhere does Nakayama et al disclose annealing to the extent that first and second semiconductor electrode regions 36 come into contact with each other as shown in Fig. 5C of the present specification. Rather, source and drain regions 12 of the NMOS transistor shown in Nakayama et al must be separated by a p-channel region; otherwise the transistor would not operate. In fact, the cited passage of Nakayama et al and all of the drawings do not show doped regions 12 coming into contact with each other. The differences are striking as shown in the comparison of Fig. 5C of the present specification with Fig. 1 of Nakayama et al reproduced below.

FIG. 5C

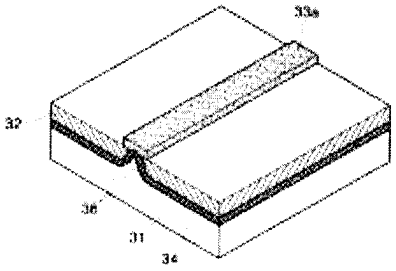
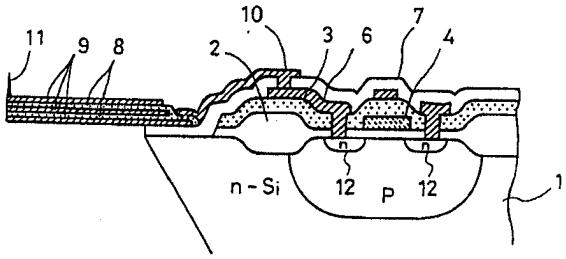


FIG. 1



Moreover, the cited passage at col. 8, lines 31-46 of Nakayama et al has no disclosure with respect to depositing a stripe-shaped photoresist in an orthogonal direction to an existing mask layer (as suggested by the Examiner) as claimed in claim 3.

With regard to claims 4 and 5, the BPSG oxide described at the cited passage at col. 8, lines 20-40 of Nakayama et al is **insulator** 3 (i.e., wiring layer 6 is formed on insulator 3), and this oxide layer is not removed *to sharpen an end point of the resistive regions* as required by present claim 4.

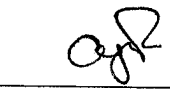
For the above reasons, it is respectfully submitted that the present claims define novel subject matter and are not anticipated by Nakayama et al, and withdrawal of the foregoing rejection under 35 U.S.C. § 102(b) is respectfully requested.

Withdrawal of all rejections and allowance of claims 1-7 is earnestly solicited.

In the event that the Examiner believes that it may be helpful to advance the prosecution of this application, the Examiner is invited to contact the undersigned at the local Washington, D.C. telephone number indicated below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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